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| 10/815,294 | 04/01/2004 | Edwin Franklin Barry | 800.0015 (A1145) | 8328 |

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| EXAMINER | |
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| DOAN, DUC T | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

mN

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/815,294 | BARRY ET AL. | |
| | Examiner | Art Unit | |
| | Duc T. Doan | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Status of Claims*

Claims 1-19 have been presented for examination in this application. Claims 1-19 are pending in this application. Claims 1-19 are rejected.

Applicant's remarks filed 10/15/2007 have been fully considered but they are not persuasive. Therefore, the rejections from the previous office action are respectfully maintained with changes as needed to address the amendments.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-6, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dowling (US 6823505) and in view of Intel Pentinum Processor Family Developer's Maunual Vol 3, hereby Intel.

As in claim 1, Dowling discloses a processor address translation apparatus for translating an instruction operand address to a different operand address (Dowling's Fig 2, processor

address translation apparatus comprises #102 register file, #150 etc..programmable address translation logic, for translating an instruction operand address, #Fig 2: #107, to a different address, see column 13, Table 5),

Dowling further discloses a memory with an address input for selecting a data element from a plurality of data element (Dowling's Fig 2: #AR0-ARn and associating auxiliary memory registers R1-RN, Dowling's column 1 lines 20-50),

Dowling's column 13, table 5 further discloses an instruction register for receiving an instruction encoded with an operand address (Table 5 instructions) and control information indicating the operand address is to be translated as part of the instruction's execution (Dowling's table 5, column 13 lines 19-35 further discloses by using the control information (i.e new "++" notation indicating address translation), the address translation apparatus translating the operand address into the translated address of the corresponding transpose element) ; and

an address translation unit for accessing the memory in a translation pattern, having the operand address as input and (Dowling's Fig 2,address translation apparatus comprising of #102, #150 etc.. accessing the memory associating with #102 AR0-Arn in a translation pattern),

Dowling further discloses in response to the instruction received in the instruction register (Dowling's Table 5 instruction), translating the operand address to form the different operand address in accordance with the translation pattern (Dowling's table 5, column 13 lines 19-35 further discloses by using the control information (i.e new "++" notation indicating address translation), the address translation apparatus translating the operand address into the translated address of the corresponding transpose element), the different operand address accessing a data element from the memory through the address input (Dowling's Fig 2, the

translated/different operand address accessing data element of memory associating with #AR0-ARN).

Dowling does not expressly disclose the claim's amended aspect of "...directly translating the operand bit field received as input .. " when doing the address translation. However, Intel discloses a typical general purpose processor with instruction having operand address expressed indirectly addressing format (Intel's page 25-6 [BX+DI] ) or direct addressing format (Intel's page 25-6 disp16). It would have been obvious to one of ordinary skill in the art at the time of invention to include operand direct addressing format as suggested by Intel in Dowling's system thus the address translation scheme can be used with direct addressing format and thereby further allowing Dowling's teaching to be used with other popular mainstream processor.

As in claim 2, Dowling further discloses several address translation functions supporting several translation patterns (Dowling's column 6 lines 47-66, programmable address translation functions supporting any desired address translation patterns such as +8, +4 etc; Dowling's column 7 lines 1-15, address translation functions for FFT algorithm, bit reversing functions or any functions for matrix calculation. Dowling Fig 5 further discloses of any translation parameters can be stored and easily programmed for processing any desired translation patterns, using well known, programmable logic devices such as PLD etc..; see Dowling's column 9 lines 40-65, PR0-PR3 etc..; column 13 lines 50 to column 14); Dowling further discloses an input to select a translation pattern from the plurality if supported translation (Dowling's column 7 lines 1-3, input that selects several addressing modes).

As in claim 4, Dowling Fig 4A, column 30-65 further discloses that the instruction is a block load instruction (i.e a typical matrix operation instruction in processor TMS320C2x).

As in claim 5, Dowling's Fig 5, in another embodiment, discloses that the processor address apparatus disposed within a plurality of instruction operand address paths (Fig 5: several instruction operand paths from dispatcher units Fig 5 #606) for a plurality of instruction, the plurality of instructions fetched for simultaneous execution (Fig 5: #617, #619 several programmable address translation functions are receiving plurality of instruction's operand addresses being fetched simultaneously).

As in claim 6, Dowling further discloses the plurality of instructions constitute a very long instruction word (VLIW) (Dowling's columns 50-56 further disclose the programmable address translation functions are incorporated into different functional and /or executing units executing instructions that constitute the VLIW instruction).

As in claim 16, Dowling discloses a processor address translation method for translating an instruction operand address to a different operand address, the address translation method comprising: receiving an instruction encoded with an operand address and control information indicating the operand address is to be translated as part of the instruction's execution; translating the operand address according to a function; and accessing a data element with the translated address (see rationale of claim 1), and repeating the receiving, translating, and accessing steps to access data elements in a pattern according to the function (Dowling's table 5, repeating steps for sequence of inputs according the function auto incrementing).

As in claim 17, Dowling further discloses wherein the function comprises combinatorial logic for translating the operand address (Dowling's column 9 lines 1-7, comprises combinational logic).

Claims 3 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dowling (US 6823505), Intel as applied to claims 2 and 16 respectively and in view of Nair et al (US 6944747).

As in claim 3, Dowling column 9, lines 40-65 discloses using the parameter registers PR0-PR3.. for providing translated addressed for automatic indexing FFT, and matrix operations (see Dowling's column 9 lines 5-15). Dowling does not expressly disclose of providing the bit complementing function for matrix operation (corresponding to the claim's e bits function). However, Nair teaches an apparatus Fig 1 to process several matrix operations (Nair's table 1 and 2), including providing bit complementing function for matrix operations, Nair's column 12 lines 13-30, bit-wise complement operation, bit-wise complement operation corresponding the claim's matrix operation with e bit). It would have been obvious to one of ordinary skill in the art at the time of invention to include bit-wise complementing function and matrix operations as suggested by Nair into Dowling's system modified by Intel , thereby the system can further providing additional complex matrix operations in an automatic manner as shown in Nair's Table 1, and 2, and thereby further improve the overall throughput in the system for executing matrix operations.

Claim 19 is rejected based on the same rationale as of claim 3.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dowling (US 6823505) and in view of Nair et al (US 6944747).

As in claim 18, Dowling discloses an address translation method for translating a first address of a first data element in a memory to a second address of a second data element in the memory (Dowling's operand address translation circuitry to translated a first address into the second address for matrix operation, see Dowling's column 7 lines 1-15, column 6 lines 47-67), the address translation method comprising:

Dowling discloses enabling an address translation unit for translation (Dowling 's column 7 lines 1-15, selecting and enabling the addressing mode for a particular address translation pattern FFT, matrix operation etc..) initiating a read operation to read a first data element at a first address during a read operation (It's is noted that any FFT, matrix operation requires reading a first source data element); translating the first address to the second address in accordance with the {s, e} bit specified translation pattern (Dowling's Fig 2,operand address translation function #212 translating address accordance with the algorithm pattern, see Dowling's column 7 lines 1-15) ; and completing the read operation by reading the second data element at the second address (Dowling's Fig 2, using the translated operand address to read the second data element that is the result of an FFT bit reserving addressing step).

Dowling does not expressly disclose the claim's detail of matrix operation with the bit complementing function. However, Nair teaches an apparatus Fig 1 to process several matrix operations (Nair's table 1 and 2), including providing bit complementing function for matrix operations, Nair's column 12 lines 13-30, bit-wise complement operation (corresponding the claim's matrix operation with e bit). It would have been obvious to one of ordinary skill in the art

at the time of invention to include bit-wise complementing function and matrix operations as suggested by Nair into Dowling's system, such that the system can further provide additional complex matrix operations as shown in Nair's Table 1, and 2 in an automatic manner, and thereby further improve the overall throughput in the system for executing matrix operations.

Nair further discloses typical matrix operation comprises of determining a set of {s, e} bits that specify a translation pattern; loading the set of {s, e} bits into an address translation parameter control register (Nair's loading the matrix parameter set of {s,e} representing by the mnemonic as shown in table 2); Dowling further discloses that any parameter set can be easily stored for operations such as matrix, FFT etc.., using well known programmable logic device PLD, see Dowling's column 14 lines 50 to column 14).

It's noted that the amended claim 18 merely rearranges some components of the address translation logic such that some of these elements are now claimed be located in "the address translation memory".

Clearly, simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination would be obvious. In this instant, Dowling's Fig 2 teaches each element of the claim's "address translation memory", and they each performing the same function it has been known to perform and yields no more than one would expect from such an arrangement (address registers 102 are used for storing addresses being translated. Data memory 120 to store corresponding data pointed to by the address in the address registers 102. Address translation is discloses by logic in 150, that including logic for parameter control logic (Dowling's Fig 3A:

PR3,PR1 that control address translation from input address registers to output address registers) thus the combination would be obvious.

Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek et al (US 6173389) and in view of Dowling (US 6823505).

As in claim 7, Pechanek discloses typically a computer system, for example a VLIW processor system, Fig 3, comprises of register file and associating register file addressing/indexing logic (i.e corresponding to the claim's RFI register file indexing logic and updating logic) to store operands in register file such that operands being stored in the register file can be quickly accessed by instruction in functional units of the processor (i.e load and store registers of register file for executing instruction such as add and multiply, see Pechanek's column 1 lines 47-61). Pechanek does not expressly disclose the logic to translate the operand addresses of sequence of instruction to an RIF sequence of different operand addresses. However, Dowling discloses an programmable address translation apparatus capable of translating a sequence of instruction operand addresses into different operand addresses of sequence of instructions (Dowling's Fig 2, column 6 lines 47-67, address register file AR0-ARn register file #102, column 13 Table 5) for several addressing translating pattern (i.e addressing modes to translate addresses of FFT patterns, and/or addressing patterns corresponding to matrices manipulation). It would have been obvious to one of ordinary skill in the art at the time of invention to include translation operand addresses into different operand addresses as suggested by Dowling such that instructions can be completed faster and thereby further improve the overall system's throughput (see Dowling's column 13 lines 19-50).

Dowling further discloses a memory with an address input for selecting a data element from a plurality of data element (Dowling's Fig 2: #AR0-ARn and associating auxiliary memory registers R1-RN, Dowling's column 1 lines 20-50),

Dowling's column 13, table 5 further discloses an instruction register for receiving an instruction encoded with an operand address (Table 5 instructions) and control information indicating the operand address is to be translated as part of the instruction's execution (Dowling's table 5, column 13 lines 19-35 further discloses by using the control information (i.e new "++" notation indicating address translation), the address translation apparatus translating the operand address into the translated address of the corresponding transpose element) ;

Although Pechanek's Fig 3 discloses a VLIW processor system having RFI, register file and associating updating logic, Pechanek does not expressly discloses the claim's detail of the associating logic to manipulate operand addresses. However, Dowling further discloses a logic that manipulates operand addresses (i.e manipulating operand addresses corresponding to address register files, Dowling's Fig 2: #AR0-ARn and associating auxiliary memory registers R1-RN, Dowling's column 1 lines 20-50), capable of generate on the register file update unit's output a linear sequence of register file operand addresses in response to received sequence of register file translation type instruction (Dowling's column 2 lines 40-50, translating operand addresses using linear auto incrementing mode).

Dowling further discloses a multiplexer for selecting between the operand address from the instruction register for a first register file operation and subsequence register file operations (Dowling's Fig 2: for selecting not translated the operand address, therefore address from the instruction register #107 or translated operand address from the programmable address

translation circuitry #212. It's further note that for incrementing addresses pattern, the first address is not being translated, and the subsequent addresses are translated to +8, -4 etc.. see Dowling's column 2 lines 50-58, thus a multiplexer is required for bypassing/not using the address translation function #217; Dowling's column 9 lines 1-15, teaches by providing feedback path of translated operand addresses (i.e output of translation function #217) to the registers #102, using for example multiplexer circuitry #203, to implement sequential logic functions. In other words, Dowling clearly teaches of using multiplexer to provide addresses not being translated, and to provide translated addresses for subsequent cycles);

Dowling further discloses an address translation unit for access the memory in a translation pattern, receiving a sequence of operand address from the multiplexer (Fig 2: #203 multiplexer feeding back path of translating addresses to the registers #102 and proving them to address translation function #212 in subsequent cycles) and in response to the sequence of RFI operand addresses, translating the sequence of RFI operand addresses to form a sequence of different operand addresses (Dowling's column 9 lines 1-15, teaches by providing feedback path of translated operand addresses (i.e output of translation function #217) to the registers #102, using for example multiplexer circuitry #203, to implement sequential logic functions. In other words, Dowling clearly teaches of using multiplexer to provide addresses not being translated, and to provide translated addresses for subsequent cycles); in accordance with the translation pattern (Dowling's table 5, column 13 lines 19-35 further discloses by using the control information (i.e new "++" notation indicating address translation), the address translation apparatus translating the operand address into the translated address of the corresponding transpose element), the different operand addresses each accessing a data element from the

memory through the address input (Dowling's Fig 2, the translated/different operand address accessing data element of memory #AR0-Arn).

As in claim 8, Dowling's Fig 5 further discloses the RFI address translation apparatus disposed within PEs of an array of PEs (Dowling: Fig 6A array of PEs comprise address translation apparatus representing by #617, #619).

As in claim 9, Dowling's Fig 6A further discloses the processor RFI address translation apparatus of claim 7 disposed within a plurality of instruction operand address paths for a plurality of instructions, the plurality of instructions fetched for simultaneous execution( Fig 6A).

As in claim 10, Dowling further discloses the processor RFI address translation apparatus of claim 9 wherein the plurality of instructions constitute a very long instruction word (VLIW) (Dowling's column 50-56 further discloses the programmable address translation functions are incorporated into different functional and /or executing units that executing instructions that constitute the VLIW instruction).

Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dowling (US 6823505) and in view of Choquette et al (US 2002/0199084).

As in claim 11, Dowling discloses an address translation memory device for accessing data at translated addresses, the address translation memory device comprising (Dowling's Fig 2, processor address translation apparatus comprises #102 register file, #150 etc..programmable address translation logic, for translating an instruction #Fig 2: #`107 operand address to a different address, see column 13, Table 5): a first read address input (Dowling's Fig 2: a first read input for reading operand address from instruction Fig 2: #107);

Although Dowling Fig 2, column 1 lines 40-45 discloses a register file structures comprises of address registers Fig 2: #AR0 that provide addresses to associating operand data stored in memory/auxiliary registers R1-Rn (corresponding to the claim's storage device). Dowling does not expressly disclose the claim's aspect of ports associating with the storage device. However, Choquette discloses a typical computer system having several execution units that operate parallel and using a register file structure Fig 1: #30. In such a system, the register file structure Fig 1: #30 (corresponding to the claim's storage device) capable of providing several read, write address ports, and several data in data out ports so that several execution units can access the file register concurrently (Choquette's paragraph 4). It would have been obvious to one of ordinary skill in the art at the time of invention to include the register file structure with several read, write address ports and several data in data out ports so that several execution units can executing and accessing the file register structure concurrently, and thereby improve the overall system's throughput (Choquette's paragraphs 1,4).

Dowling further discloses the operand address translation apparatus for accessing the storage device in a translation pattern, the address translation unit translating the first read address input in accordance with the translation pattern (Dowling's Fig 2: # 3217 programmable address translation function translates address in accordance with translation pattern, auto increment or FFT etc.., see Dowling's column 6 lines 45 to column 7 line 15), to the storage device second read address input for reading data from the storage device at a translated address during read operation (Again, it's further noted as disclosed by Choquette in above paragraph, several storage ports (read write addresses data ports are provided so that the register file can be accessed by several executing units concurrently).

It's noted that the amended claim 11 merely rearranges some components of the address translation logic such that some of these elements are now claimed be located in "the address translation memory".

Clearly, simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination would be obvious. In this instant, the recited references teach each elements of the claim's "address translation memory device", and they each performing the same function it has been known to perform and yields no more than one would expect from such an arrangement (address registers 102 are used for storing addresses being translated. Data memory 120 to store corresponding data pointed to by the address in the address registers 102. Address translation is discloses by logic in 150, that including logic for parameter control logic (Dowling's Fig 3A: PR3,PR1 that control address translation from input address registers to output address registers) thus the combination would be obvious.

Claim 12 discloses a variation of claim 11, and directs to a write operation. The claim is rejected based on the same rationale as of claim 11. Again, it's further noted as disclosed by rationale in claim 11, several storage ports, read, write, addresses, and data ports are provided so that the register file can be accessed in either read or write operations by several executing units in a concurrently manner.

As in claim 13, Dowling's Fig 2 clearly discloses processor address translation apparatus comprises #102 register file, #150 etc..programmable address translation logic, for translating an instruction #Fig 2: #107 operand address to a different address, see column 13, Table 5; Dowling

further discloses wherein the storage device (auxiliary register R0-Rn) having location selection logic (Fig 2: #AR0-AR) merging with the address translation unit (Fig 2: #217).

Claim 14 is rejected based on the same rationale as of claim 2.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dowling (US 6823505), Choquette et al (US 2002/0199084) as applied to claim 14, and further in view of Nair et al (US 6944747).

As in claim 15, none of Dowling and Choquette discloses the claim's aspect of complementing bit function of matrix operation. However Nair teaches the claim's limitation as discussed in the rationale of claim 3.

***Response to Arguments***

The applicant's arguments filed 10/15/2007 have been fully considered as follow:

A) Applicant's amendment to the Abstract overcomes the Specification Objection in the previous Office Action.

B) Applicant's arguments regarding the rejections of claims 1,2,4-6, and 17 under 35 U.S.C 102(e) are not persuasive.

As to the amended claim 1, the amended claim appears to describe an instruction having the operand address in direct addressing format. That is the operand address bit field corresponds to memory location. Dowling does not expressly disclose the direct addressing format of the operand address. However Intel clearly discloses a typical general purpose computer having the operand address in direct addressing format (Intel's page 25-6 disp16). It would have been

obvious to one of ordinary skill in the art at the time of invention to include operand direct addressing format as suggested by Intel in Dowling's system thus the address translation scheme can be used with direct addressing format and thereby further allowing Dowling's teaching to be used in several types of computer systems.

As to Applicant's arguments regarding the rejection of claim 4, Applicant argues that Dowling does not disclose the block load instruction. Examiner disagrees, Dowling's Fig 4A, column 10 lines 30-65, discloses an matrix operation that load data elements from memory into registers, the data element can be word, double words etc ..that represent a block of data. Therefore Applicant's argument is not persuasive.

As to Applicant's arguments regarding the rejection of claim 16, Applicant relies on a similar argument as presented above regarding claim 1. Accordingly, Examiner maintains the rejection of this claim and its dependent claims under the same reasoning presented above.

As to Applicant's arguments regarding the rejection of claims 3,18 and 19 under 35 U.S.C 103(a), Applicant argues "Nair does not describe operations that can be performed on an "operand address bit field input". The argument is not persuasive. Nair teaches a mechanism to manipulate bit complementing function for matrix operation. The "bit" in Nair represents any type of data bit that is required by the application using the bit complementing function. Thus Nair's bit can represent an address value when the application using the bit as address bit. Therefore Nair's teaching of bit complementing function is readily to be applied in Dowling's address translation scheme and wherein Nair's bit represents "operand address bit field input" as designated in Dowling's system. Thus Applicant's argument is not persuasive.

As to Applicant's arguments regarding the rejection of the amended claim 18, applicant argues that "Dowling's data memory 102 is not an address translation memory". The argument is not understood. Dowling's data memory 102 have the data correspond to the address registers AR0 to ARn. These address registers contains addresses that used for address translation, and thus belong to "the address translation memory". Applicant's remaining arguments are not relevant because they are based on the false assumption that Dowling's data memory is the claim's address translation memory.

It's noted that the amended claim 18 merely rearranges some components of the address translation logic such that some of these elements are now claimed be located in "the address translation memory".

Clearly, simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination would be obvious. In this instant, Dowling's Fig 2 teaches each element of the claim's "address translation memory", and they each performing the same function it has been known to perform and yields no more than one would expect from such an arrangement (address registers 102 are used for storing addresses being translated. Data memory 120 to store corresponding data pointed to by the address in the address registers 102. Address translation is discloses by logic in 150, that including logic for parameter control logic (Dowling's Fig 3A: PR3,PR1 that control address translation from input address registers to output address registers) thus the combination would be obvious. Therefore Applicant's arguments are not persuasive.

As to Applicant's arguments regarding the rejection of the claims 7-10, Applicant alleges that Penachek does not teach the register file indexing logic and updating logic. However,

Applicant fails to set forth differences between each claims' elements and the teaching of recited references as stated in the rejection of the claims.

C) As to Applicant's arguments regarding the rejection of the claims 11-14 under 35 U.S.C 103(a)

Applicant's arguments regarding claims 11-14 are similar to the arguments offered for claim 18 and the same responses apply (see response in item B above).

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER

12/20/07